

e : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.	2 Any revealing of identification, appeal to evaluator and /or equations written eg. $42+8 = 50$, will be treated as malpractice.
30 u	7
ō	A
_;	C
 •	

-	S7	5) ver	n	V	LS _	SI —	2)eg	,iq	$n \not$	7	_m	be	dd	ed	Si	/8t	em	rs				
USN																	- •				12	EC	129)

M.Tech. Degree Examination, February 2013

SoC Design

Time: 3 hrs.	Max. Marks: 100

Note: Answer any FIVE full questions.

1	a. b. c.	What are the typical goals of SoC design? Write briefly how it is achieved. Compare SoC, SiP and SoB on different characteristics. Differentiate between hard IP, soft IP and firm IP with an example.	(10 Marks) (06 Marks) (04 Marks)
	С.	Differentiate between hard if, soft if and firm if with an example.	(04 Marks)
2	a. b.	Explain with a diagram spiral and waterfall model of SoC system design. What are the importance of specifications in SoC design process? Explain	(10 Marks) types of
		specification.	(07 Marks)
	c.	What are the characteristics of good IP?	(03 Marks)
3	a.	Explain various system level design issues in SoC design.	(08 Marks)
	b.	Explain with flow diagram, the SoC system process.	(08 Marks)
	c.	What is timing closure problem? State two methods of over coming timing closure	problem. (04 Marks)
4	a.	Explain working of NAND FLASH memory.	(05 Marks)
	b.	What is cache coherence? Explain MESI protocol for coherence problem.	(10 Marks)
	c.	What are the different low power techniques used in SoC design?	(05 Marks)
5	a.	Discuss limitations of bus based architecture with NOC topologies. What are the	properties
		of NOC topologies?	(08 Marks)
	b.	What are different switching strategies in NOC? Explain worm hole switching.	(07 Marks)
	c.	Why routing algorithm required in NOC?	(05 Marks)
6	a.	What and why MPSOC?	(06 Marks)
•	b.	What are the challenges in designing MPSOC?	(08 Marks)
	c.	Discuss techniques used to reduce stand by energy in process architecture and mer	nory.
	٠.	- The state of the	(06 Marks)
7	a. b.	Discuss energy aware ON chip communication system design techniques. What are the advantages of design migration from FSM controlled RTL design	(08 Marks) gn to firm
		controlled configurable and extensible system design?	(08 Marks)
	c.	Write a program in TIE language to add a new register file and a new instruc xtensa processor.	(04 Marks)

(10 Marks) (05 Marks) Write a note on XTMP.

(05 Marks) c. Write a note on hardware accelerator.

Discuss various aspects of low power open multimedia application platform for 3G wireless.